CLAIMS

What is claimed is:

1. A system routing a data structure to facilitate error correction, the system comprising:

a data structure partitioned into a plurality of adjacent bit pair domains, such that a single adjacent bit pair from each of a plurality of memory devices is assigned to an adjacent bit pair domain for each of the plurality of adjacent bit pair domains; and

a data router that transmits adjacent bit pair domain data over a bus having a plurality of data paths, the data router transmits a first set of bits associated with a respective adjacent bit pair domain during a first transfer cycle, and transmits a second set of bits associated with the respective adjacent bit pair domain during a second transfer cycle, such that bits associated with a given adjacent bit pair are transmitted over a same data path for the plurality of data paths.

2. The system of claim 1, the first set of bits being associated with one of a same even column and odd column of the plurality of memory devices, and the second set of bits being associated with the other of the even column and odd column of the plurality of memory devices.

3. The system of claim 1, the data router repeats the transmission of a first set of bits during a first transfer cycle and a second set of bits during a second transfer cycle for each of the plurality of adjacent bit pair domains, such that bits associated with a given memory device are transmitted over a same data path over a plurality of first and second transfer cycles.

4. The system of claim 1, further comprising:

a domain data aggregator that aggregates the first set of bits and the second set of bits to reconstruct the respective adjacent bit pair domain; and

an error detection and correction (EDC) component that detects and corrects errors associated with the reconstructed adjacent bit pair domain.

5. The system of claim 4, the EDC component detects and corrects errors associated with the plurality of adjacent bit pair domains in a one of a sequential manner and a parallel manner.

6. The system of claim 1, the data router being a buffer/multiplexer device.

7. The system of claim 1, the data structure comprising B bits and the plurality of adjacent bit pair domains having B/2 bits, where B is an integer multiple of four that is greater than or equal to eight.

8. The system of claim 7, the data structure comprising 288 bits and each of the plurality of adjacent bit pair domains having 144 bits.

9. The system of claim 1, the data structure having K * W bits, where K is the number of the plurality of memory devices forming a system memory, and W is the column widths of the plurality of memory devices.

10. The system of claim 1, further comprising a check bit generator that generates check bits that are aggregated with data bits to form an adjacent bit pair domain for each of the plurality of adjacent bit pair domains.

11. A server comprising the system of claim 1.

12. The system of claim 1 being configured to enable chipkill functionality for the plurality of memory devices and the plurality of data paths.

13. A memory system comprising:

a plurality of memory devices operative to store a data structure over the plurality of memory devices corresponding to a given memory address;

a buffer/multiplexer device that transmits and receives the data structures over a first bus and transmits and receives adjacent bit pair domain data over a second bus, the second bus having a plurality of data paths associated therewith, the adjacent bit pair domain data comprising a single adjacent bit pair from each of a plurality of

memory devices assigned to an adjacent bit pair domain for a plurality of adjacent bit pair domains, the adjacent bit pair domain data being transmitted over the second bus, such that adjacent bit pairs associated with a given memory device are transmitted over a same data path; and

a controller operative to transmit and receive adjacent bit pair domain data over the second bus and operative to transmit and receive data blocks corresponding to the adjacent bit pair domain data over a third bus.

14. The system of claim 13, the buffer/multiplexer device transmits a first set of bits associated with a respective adjacent bit pair domain over the second bus during a first transfer cycle, and a second set of bits associated with the respective adjacent bit pair domain over the second bus during a second transfer cycle, such that bits associated with a single adjacent bit pair are transmitted over a same data path in a two cycle transfer.

15. The system of claim 14, the buffer/multiplexer device repeats the transmission of a first set of bits during a first transfer cycle and a second set of bits during a second transfer cycle for each of the plurality of adjacent bit pair domains, such that bits associated with a given memory device are transmitted over a same data path over a plurality of two cycle transfers.

16. The system of claim 14, the controller further comprising:

a domain data aggregator that aggregates the first set of bits and the second set of bits to reconstruct the adjacent bit pair domain; and

an error detection and correction (EDC) component operative to detect and correct single bit errors and adjacent double bit errors associated with a respective adjacent bit pair domain.

17. The system of claim 13, the controller being one of a memory controller and a cache coherency controller.

18. The system of claim 13, the controller further comprising a check bit generator that generates check bits associated with respective adjacent bit pair

domains, the check bits being employed by an EDC component to correct single bit errors and adjacent double bit errors.

19. A system for routing a data structure to facilitate error correction, the system comprising:

means for partitioning a data structure into a plurality of adjacent bit pair domains, each adjacent bit pair domain being populated with a single adjacent bit pair from each of a plurality of memory devices associated with a given memory address;

means for detecting and correcting single bit errors and adjacent double bit errors associated with a respective adjacent bit pair domain; and

means for routing the adjacent bit pair domain data over a bus having a plurality of data paths to the means for detecting and correcting, the means for routing transmitting single adjacent bit pairs associated with respective memory devices over respective same data paths of the plurality of data paths.

20. The system of claim 19, the means for routing transmitting a first set of bits during a first cycle and a second set of bits during a second cycle for a respective adjacent bit pair domain, such that bits associated with a given adjacent bit pair and a given memory device are transmitted over a same data path over a two cycle transfer for each of the plurality of adjacent bit pair domains.

21. The system of claim 19, the means for detecting and correcting comprising a plurality of means for detecting and correcting single bit errors and adjacent double bit errors associated with different respective adjacent bit pair domains.

22. A method of routing a data structure to facilitate the detection and correction of errors, the method comprising:

reading a data structure from a plurality of memory devices associated with a given memory address;

separating the data structure into a plurality of adjacent bit pair domains, each adjacent bit pair domain being populated with a single adjacent bit pair from each of a plurality of memory devices associated with a given memory address;

transmitting adjacent bit pair domain data associated with the plurality of adjacent bit pair domains over a bus having a plurality of data paths, the adjacent bit pair domain data associated with a respective adjacent bit pair domain being transmitted over the bus in a two-cycle transfer, such that bits associated with a given memory device are transmitted over a same data path;

aggregating the adjacent bit pair domain data associated with the two-cycle transfer to reconstruct the respective adjacent bit pair domain; and

performing error detection and correction on the reconstructed respective adjacent bit pair domain.

23. The method of claim 22, further comprising repeating the two-cycle transfer for each of the plurality of adjacent bit pair domains, such that bits associated with a given memory device from each of the plurality of adjacent bit pair domains are transmitted over a same data path.

24. The method of claim 22, the performing error detection and correction comprising performing error detection and correction to correct for single bit errors and adjacent double bit errors in the reconstructed respective adjacent bit pair domain.

25. The method of claim 22, the transmitting adjacent bit pair domain data over the bus in a two-cycle transfer, such that bits associated with a given memory device are transmitted over a same data path enables chipkill functionality for the plurality of memory devices and the plurality of data paths.